ML4026-56-0dB-3.5W

MSA Compliant SFP56

Electrical Passive Loopback Interconnect

multiLane

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ML4026-56-0dB-3.5W Electrical Passive Loopback Interconnect - Key Features

- ✓ Power Consumption up to 3.5W
- ✓ Operation up to 56Gb/s per lane
- ✓ Dual LED indicator
- ✓ Custom Memory Maps
- ✓ 100% at rate AC testing
- ✓ Temperature range from -5° to 85° C
- ✓ MSA Compliant EEPROM
- ✓ Voltage sense
- ✓ Current sense
- ✓ Temperature sense
- ✓ Insertion Counter
- ✓ Automatic shut down and self-protection
- ✓ Micro controller based

➢ LED Indicator

GREEN - Signifies that the module is fully plugged-in and operating in high power permitted mode.

RED - Signifies the module is fully plugged-in and operating in low power mode.

BLINKING - Signifies any of the interrupt flags is set

➢ Operating Conditions

Recommended Operation Conditions						
Parameter	**Symbol**	**Notes/Conditions**	**Min**	**Typ**	**Max**	**Units**
Operating Temperature	T_A		-5		85	°C
Supply Voltage	VCC	Main Supply Voltage	3.00	3.3	3.60	V
Data Rate	R_b	Guaranteed to work at 56 Gbps per lane	0		56	Gbps
Input/Output Load Resistance	RL	AC-Coupled, Differential	90	100	110	Ω
Power Class		Programmable to Emulate all power classes	0		3.5	W

1. General Description

The **ML4026-56-0dB-3.5W** SFP56 Passive Electrical Loopback is used for testing SFP56 transceiver ports under board level tests. Substituting a fully featured SFP56 transceiver with the **ML4026-56-0dB-3.5W** in loopback provides a cost effective low loss method for SFP56 port testing.

The **ML4026-56-0dB-3.5W** is packaged in a standard MSA housing compatible with all SFP56 ports. High speed signals are electrically lopped back from TX side to RX side of the module, the differential TX pair is connected to the corresponding RX pair, and the signals are AC coupled as specified by SFP MSA HW specs.
It provides an economical way to exercise SFP56 ports during R&D validation, production testing, and field testing.

The **ML4026-56-0dB-3.5W** provides SFP56 power Class 1, 2, 3 (standard), or 4 loading using a customer supplied +3.3V voltage supply.

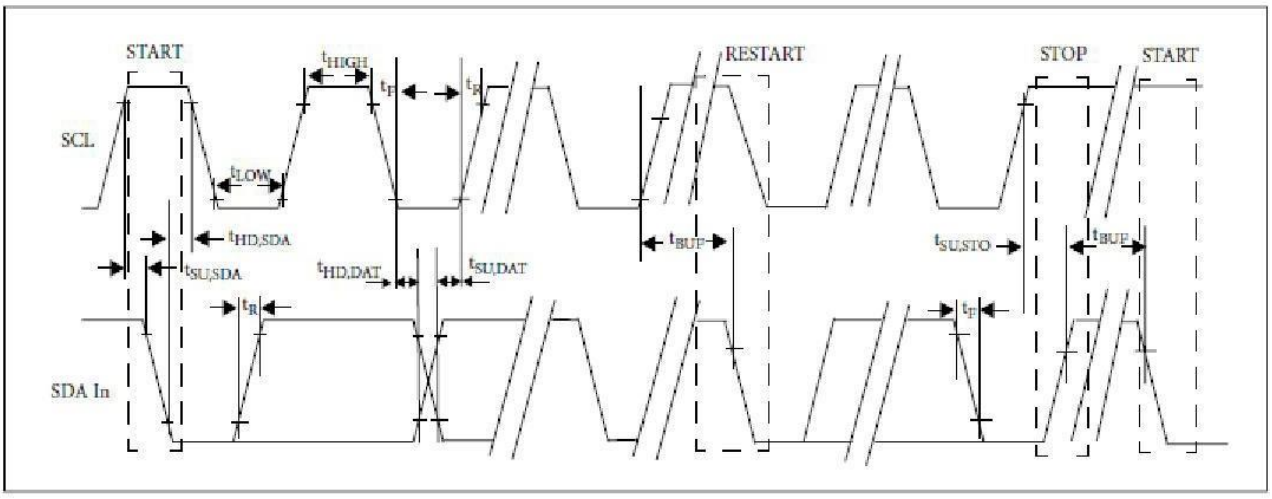
2. Functional Description

2.1 Serial Data Interface – I2C

The ML4026-56-0dB-3.5W supports the I2C interface. This SFP specification is based on the SFF8472.

2.2 I2C Signals, Addressing and Frame Structure

I2C Frame:



The 2-wire serial interface address of the SFP56 module is A0h or A2h.

Parameter	Symbol	Min	Max	Unit
Clock Frequency	f_{SCL}	30	400	kHz
Clock Pulse Width Low	t_{LOW}	1.2		us
Clock Pulse Width High	t_{High}	1.1		us
Time bus free before new transmission can start	t_{BUF}	20.8		us
Input Rise Time (400kHz)	$t_{R,400}$	300		ns
Input Fall Time (400kHz)	$t_{F,400}$	300		ns
Serial Interface Clock Holdoff "Clock Stretching"	T_{clock_hold}		500	us

Clock and Data Transitions: The SDA pin is normally pulled high with an external device. Data on the SDA pin may change only during SCL low time periods. Data changes during SCL high periods indicate a START or STOP condition. All addresses and data words are serially transmitted to and from the SFP56 in 8-bit words. Every byte on the SDA line must be 8-bits long. Data is transferred with the most significant bit (MSB) first.

START Condition: A high-to-low transition of SDA with SCL high is a START condition, which must precede any other command.

STOP Condition: A low-to-high transition of SDA with SCL high is a STOP condition.

Acknowledge: After sending each 8-bit word, the transmitter releases the SDA line for one bit time, during which the receiver is allowed to pull SDA low (zero) to acknowledge (ACK) that it has received each word. Device address bytes and write data bytes initiated by the host shall be acknowledged by SFP56 transceivers. Read data bytes transmitted by SFP56 transceivers shall be acknowledged by the host for all but the final byte read, for which the host shall respond with a STOP instead of an ACK.

Memory (Management Interface) Reset: After an interruption in protocol, power loss or system reset the SFP56 management interface can be reset. Memory reset is intended only to reset the SFP56 transceiver management interface (to correct a hung bus). No other transceiver functionality is implied.

1. Clock up to 9 cycles
2. Look for SDA high in each cycle while SCL is high
3. Create a Start condition as SDA is high

Device Addressing: SFP56 devices require an 8-bit device address word following a start condition to enable a read or write operation. The device address word consists of a mandatory sequence for the first seven most significant bits of device address (A0h or A2h). This is common to all SFP56 devices.

The eighth bit of the device address is the read/write operating select bit. A read operation is initiated if this bit is set high and a write operation is initiated if this bit is set low.

2.3 I2C Read/Write Functionality

2.3.1 SFP56 Memory Address Counter (Read AND Write Operations)

SFP56 devices maintain an internal data word address counter containing the last address accessed during the latest read or write operation, incremented by one. The address counter is incremented whenever a data word is received or sent by the module. This address stays valid between operations as long as SFP56 power is maintained. The address "roll over" during read and writes operations is from the last byte of the 128-byte memory page to the first byte of the same page.

2.3.2 Read Operations

2.3.2.1 Current Address Read

A current address read operation requires only the device address read word (10100001) be sent, see Figure 1 below.

		< -- SFP+ ADDRESS ->																		
HOST	START	MSB						LSB	READ									NACK	STOP
		1	0	1	0	0	0	x	1	0	x	x	x	x	x	x	x	1	
SFP+										ACK	MSB						LSB		
											<----- DATA WORD ----->								

Figure 1: SFP56 Current Address Read Operation

Once acknowledged by the SFP56, the current address data word is serially clocked out. The host does not respond with an acknowledgement, but does generate a STOP condition once the data word is read.

2.3.2.2 Random Read

A random read operation requires a "dummy" write operation to load in the target byte address as shown in Figure 2 below. This is accomplished by the following sequence.

		< -- SFP+ ADDRESS ->									<- MEMORY ADDRESS ->									< -- SFP+ ADDRESS -->																		
HOST	START	MSB							LSB	WRITE		MSB							LSB		START	MSB						LSB	READ									NACK	STOP
		1	0	1	0	0	0	x	0	0	x	x	x	x	x	x	x	x	0		1	0	1	0	0	0	x	1	0	x	x	x	x	x	x	x	x	1	
SFP+										ACK									ACK									ACK	MSB							LSB			
																													<---- DATA WORD ---->									

Figure 2: SFP56 Random Read

The target 8-bit data word address is sent following the device address write word (10100000) and acknowledged by the SFP56. The host then generates another START condition (aborting the dummy write without incrementing the counter) and a current address read by sending a device read address (10100001). The SFP56 acknowledges the device address and serially clocks out the requested data word. The host does not respond with an acknowledgement, but does generate a STOP condition once the data word is read.

2.3.2.3 Sequential Read

Sequential reads are initiated by a current address read (Figure 3). To specify a sequential read, the host responds with an acknowledgement (instead of a STOP) after each data word. As long as the SFP56 receives an acknowledgement, it shall serially clock out sequential data words. The sequence is terminated when the host responds with a NACK and a STOP instead of an acknowledgement.

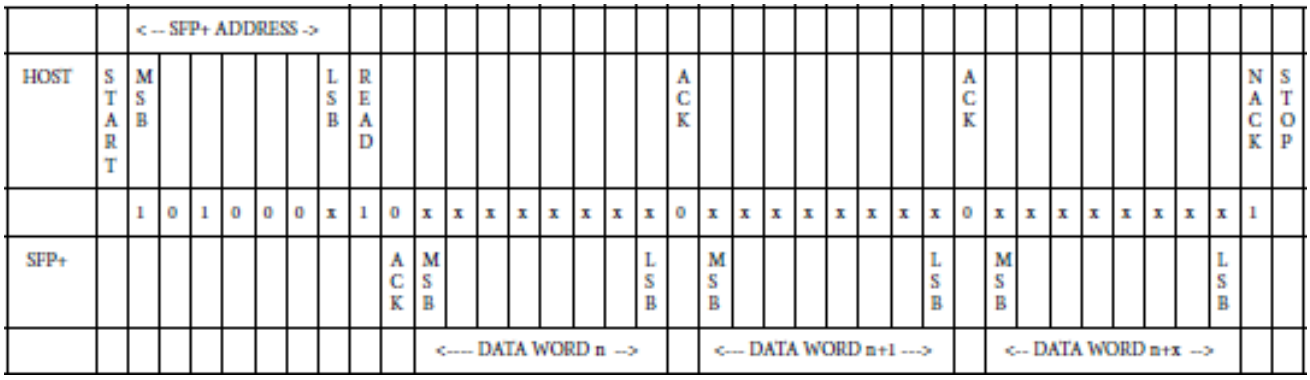


Figure 3: Sequential Address Read Starting at SFP56 Current Address

2.4 SFP56 Memory Map

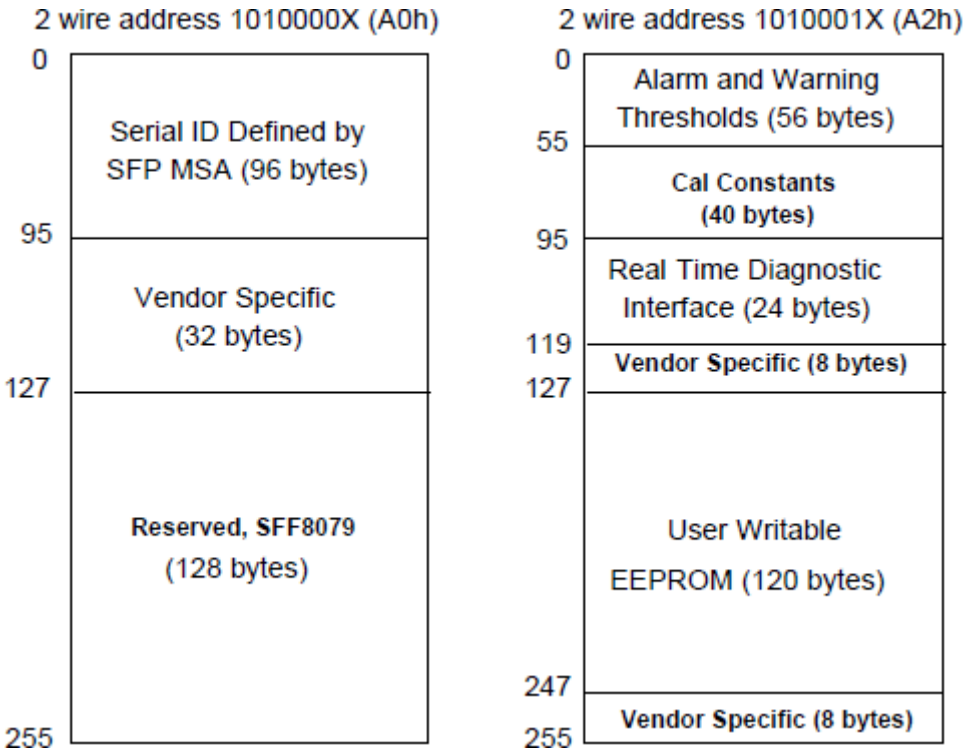


Figure 4: SFP56 Memory Map

Data Address	Size (Bytes)	Name of Field	Description of Field
BASE ID FIELDS			
0	1	Identifier	Type of transceiver (see Table 3.2)
1	1	Ext. Identifier	Extended identifier of type of transceiver (see Table 3.3)
2	1	Connector	Code for connector type (see Table 3.4)
3-10	8	Transceiver	Code for electronic or optical compatibility (see Table 3.5)
11	1	Encoding	Code for high speed serial encoding algorithm (see Table 3.6)
12	1	BR, Nominal	Nominal signalling rate, units of 100MBd.
13	1	Rate Identifier	Type of rate select functionality (see Table 3.6a)
14	1	Length(SMF,km)	Link length supported for single mode fiber, units of km
15	1	Length (SMF)	Link length supported for single mode fiber, units of 100 m
16	1	Length (50um)	Link length supported for 50 um OM2 fiber, units of 10 m
17	1	Length (62.5um)	Link length supported for 62.5 um OM1 fiber, units of 10 m
18	1	Length (cable)	Link length supported for copper or direct attach cable, units of m
19	1	Length (OM3)	Link length supported for 50 um OM3 fiber, units of 10 m
20-35	16	Vendor name	SFP vendor name (ASCII)
36	1	Transceiver	Code for electronic or optical compatibility (see Table 3.5)
37-39	3	Vendor OUI	SFP vendor IEEE company ID
40-55	16	Vendor PN	Part number provided by SFP vendor (ASCII)
56-59	4	Vendor rev	Revision level for part number provided by vendor (ASCII)
60-61	2	Wavelength	Laser wavelength (Passive/Active Cable Specification Compliance)
62	1	Unallocated	
63	1	CC_BASE	Check code for Base ID Fields (addresses 0 to 62)
EXTENDED ID FIELDS			
64-65	2	Options	Indicates which optional transceiver signals are implemented (see Table 3.7)
66	1	BR, max	Upper bit rate margin, units of %
67	1	BR, min	Lower bit rate margin, units of %
68-83	16	Vendor SN	Serial number provided by vendor (ASCII)
84-91	8	Date code	Vendor's manufacturing date code (see Table 3.8)
92	1	Diagnostic Monitoring Type	Indicates which type of diagnostic monitoring is implemented (if any) in the transceiver (see Table 3.9)
93	1	Enhanced Options	Indicates which optional enhanced features are implemented (if any) in the transceiver (see Table 3.10)
94	1	SFF-8472 Compliance	Indicates which revision of SFF-8472 the transceiver complies with. (see Table 3.12)
95	1	CC_EXT	Check code for the Extended ID Fields (addresses 64 to 94)
VENDOR SPECIFIC ID FIELDS			
96-127	32	Vendor Specific	Vendor Specific EEPROM
128-255	128	Reserved	Reserved for SFF-8079

Figure 5: Two-wire interface ID Data fields-Address A0h

Data Address	Size (Bytes)	Name of Field	Description of Field
DIAGNOSTIC AND CONTROL/STATUS FIELDS			
0-39	40	A/W Thresholds	Diagnostic Flag Alarm and Warning Thresholds (see Table 3.15)
40-55	16	Unallocated	
56-91	36	Ext Cal Constants	Diagnostic calibration constants for optional External Calibration (see Table 3.16)
92-94	3	Unallocated	
95	1	CC_DMI	Check code for Base Diagnostic Fields (addresses 0 to 94)
96-105	10	Diagnostics	Diagnostic Monitor Data (internally or externally calibrated) (see Table 3.17)
106-109	4	Unallocated	
110	1	Status/Control	Optional Status and Control Bits (see Table 3.17)
111	1	Reserved	Reserved for SFF-8079
112-113	2	Alarm Flags	Diagnostic Alarm Flag Status Bits (see Table 3.18)
114-115	2	Unallocated	
116-117	2	Warning Flags	Diagnostic Warning Flag Status Bits (see Table 3.18)
118-119	2	Ext Status/Control	Extended module control and status bytes (see Table 3.18a)
GENERAL USE FIELDS			
120-127	8	Vendor Specific	Vendor specific memory addresses (see Table 3.19)
128-247	120	User EEPROM	User writable non-volatile memory (see Table 3.20)
248-255	8	Vendor Control	Vendor specific control addresses (see Table 3.21)

Figure 6: Diagnostics Data fields-Address A2h

2.5 ML4026-56-0dB-3.5W Specific Functions

2.5.1 Temperature Monitor

The ML4026-56-0dB-3.5W has an internal temperature sensor in order to continuously monitor the module temperature. The temperature sensor readings are present in low-memory registers 96-97 as specified by SFF8472. Internally measured Module temperature are represented as a 16-bit signed two's complement value in increments of 1/256 degrees Celsius, yielding a total range of –128C to +128C that is considered valid between –40 and +125C. Temperature monitoring resolution is better than 1 degC.

Address	Bit	Name	Description
96	ALL	Temperature MSB	Internally measured module temperature
97	ALL	Temperature LSB	Internally measured module temperature

2.5.2 Insertion Counter

The Insertion counter contains the number of times the module was plugged in a host. The insertion counter is incremented every time the module goes in initializing sequence, as it is nonvolatile it is always saved. The insertion counter can be read from registers 130-131 at slave address A2h.

Address	Bit	Name	Description
130	ALL	Insertion Counter MSB	Number of times the modules was plugged in a host
131	ALL	Insertion Counter LSB	LSB unit => 1 insertion

2.5.3 Maximum Insertion Counter

The max insertion counter contains the maximum number of insertions allowed. Its default value is 65535. It can be read from registers 132-133 at slave address A2h.

Address	Bit	Name	Description
132	ALL	Max Insertion Counter MSB	
133	ALL	Max Insertion Counter LSB	LSB unit = 1 insertion

When the insertion count exceeds the max insertion counter, the Insertion counter flag will be set and the LED starts blinking. This flag is read from register 134 at slave address A2h.

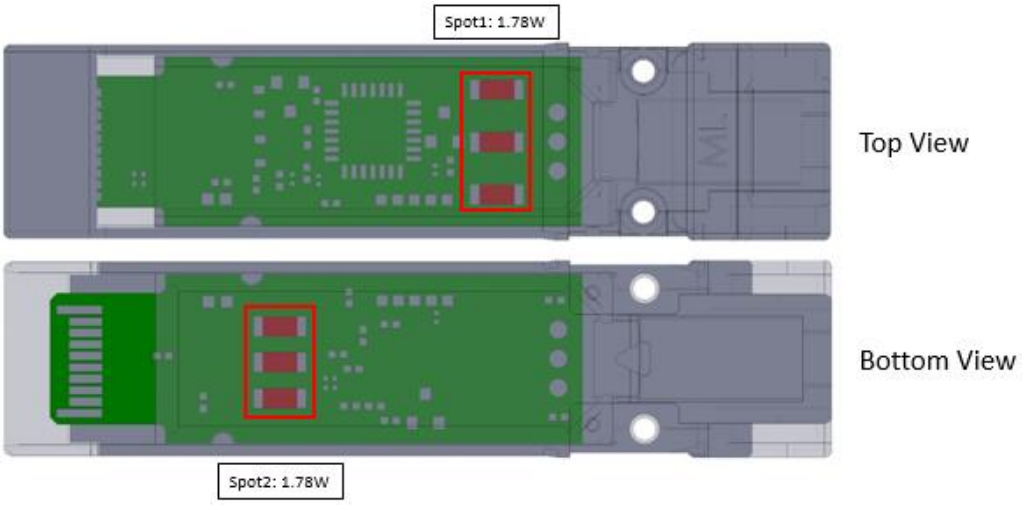
Address	Bit	Name	Description
134	0	Insertion counter flag	0: Flag not set 1: Flag Set

2.5.4 Programmable Power Dissipation & Thermal Emulation

Registers 128-129 at slave address A2h are used for PWM1 and PWM2 control over I2C. They are 8 bit data wide registers.
The consumed power changes accordingly when the value in this register is changed (only when in high power mode). In Low power mode the module automatically turns off the PWM.
The values written in these registers are permanently stored.
PWM1 and PWM2 can also be used for module thermal emulation.
The module contains 2 thermal spots positioned where the optical transceivers usually are in an optical module that is heated relative to the related PWM register. Each spot can dissipate up to 1.78W with a 6.7 mW precision.

Address	Bit	Name	Description
128	0:7	1.78W PWM controller	Power consumption varies linearly with the value set. Bits [7:0] Val = 0 to 255 corresponds to 0 to 1.78W power consumption
129	0:7	1.78W PWM controller	Power consumption varies linearly with the value set. Bits [7:0] Val = 0 to 255 corresponds to 0 to 1.78W power consumption

The power spots distribution is shown in the image below.



2.5.5 Cut-Off Temperature

To avoid overheating the module, a Cut-Off Temperature is pre-defined.
The module is continuously monitoring the temperature and checking its value against the Cut-Off temperature. Once the module temperature reaches the cut-off temperature, the PWM will automatically turn off in order to prevent overheating. Once the temperature is 5 degrees below cut-off value, the PWM goes back to its previous value.
It is read from register 144 at slave address A2h.
The Cut-Off temperature for the ML4026-56-0dB-3.5W is 85°C, and the maximum allowed is 90°C.

Address	Bit	Name	Default
144	0:7	Temperature Cut-Off	85

2.5.6 Voltage Sense

Two voltage sense circuits are available in the ML4026-56-0dB-3.5W that allows to measure the internal module supplied voltage Vcc on each of the VCC rails VCCt and VCCr. Measured values range from 0 to 6.55V. LSB unit is 100µV.

Address	Bit	Name	Description
98	ALL	VccR MSB	Internally measured module VccR
99	ALL	VccR LSB	Internally measured module VccR
Address	**Bit**	**Name**	**Description**
120	ALL	VccT MSB	Internally measured module VccT
121	ALL	VccT LSB	Internally measured module VccT

2.5.7 Status and control registers

Register 119 can be used to control Tx_fault, RX_LOS and MOD_ABS pins and Register 110 reports the digital state of the SFP low speed signals. These registers are accessed on slave address A2h.

Address	Bit	Name	Description
119	0	Tx_fault	Assert/de-assert Tx_fault pin
119	1	MOD_ABS	Assert/de-assert MOD_ABS pin
119	2	RX_LOS	Assert/de-assert RX_LOS pin
Address	Bit	Name	Description
110	4	RS(0)	Digital state of the SFP Rate Select Input Pin RS0
110	5	RS(1)	Digital state of the SFP Rate Select Input Pin RS1
110	7	Tx_Dis	Digital state of the TX Disable Input Pin

2.5.8 TX_DIS and Low Powe Mode

When Tx_disable is asserted the module enters low power mode, switches to minimal power consumption by turning off the programmable power spots, the module front LED is RED in low power mode.

When Tx_disable is de-asserted, the module is operating in high power mode, power consumption can be configured to any desired value and the module front LED is GREEN.

2.5.9 Tristate Control Signals

RS0, RS1, RX_LOS, TX_Fault and MOD_ABS signals have 56K pull-down resistors on the ML4026-56-0dB-3.5W. When tristated, those signals become pulled down by the 56K resistors and the presence of a 10K pull up resistor can be detected on the host based on the signal level (Hi/Low).

To tristate, set the corresponding bit to 1.

Address	Bits	Name	Default Value
135	0: RS0 1: RS1 2: RX_LOS 3:TX_Fault 4: MOD_ABS	Tristate Control Signal	0

2.5.10 Alarm and warning thresholds

Each A/D quantity has a corresponding high alarm, low alarm, high warning and low warning threshold. These factory preset values allow the user to determine when a particular value is outside of "normal" limits. While Voltage LSB unit is 100 µV and Temperature LSB unit is 1/256 ˚C.

A2h	Name	Default Value	Effective Value
00	High Temp Alarm Mapping (MSB)	80	80 ˚C
01	High Temp Alarm Mapping (LSB)	0	
02	LOW Temp Alarm Mapping (MSB)	0	0 ˚C
03	LOW Temp Alarm Mapping (LSB)	0	
08	High Volt Alarm Mapping (MSB)	136	3.5 V
09	High Volt Alarm Mapping (LSB)	184	
10	LOW Volt Alarm Mapping (MSB)	117	3 V
11	LOW Volt Alarm Mapping (LSB)	48	

3. ML4026-56-0dB-3.5W Pin Allocation

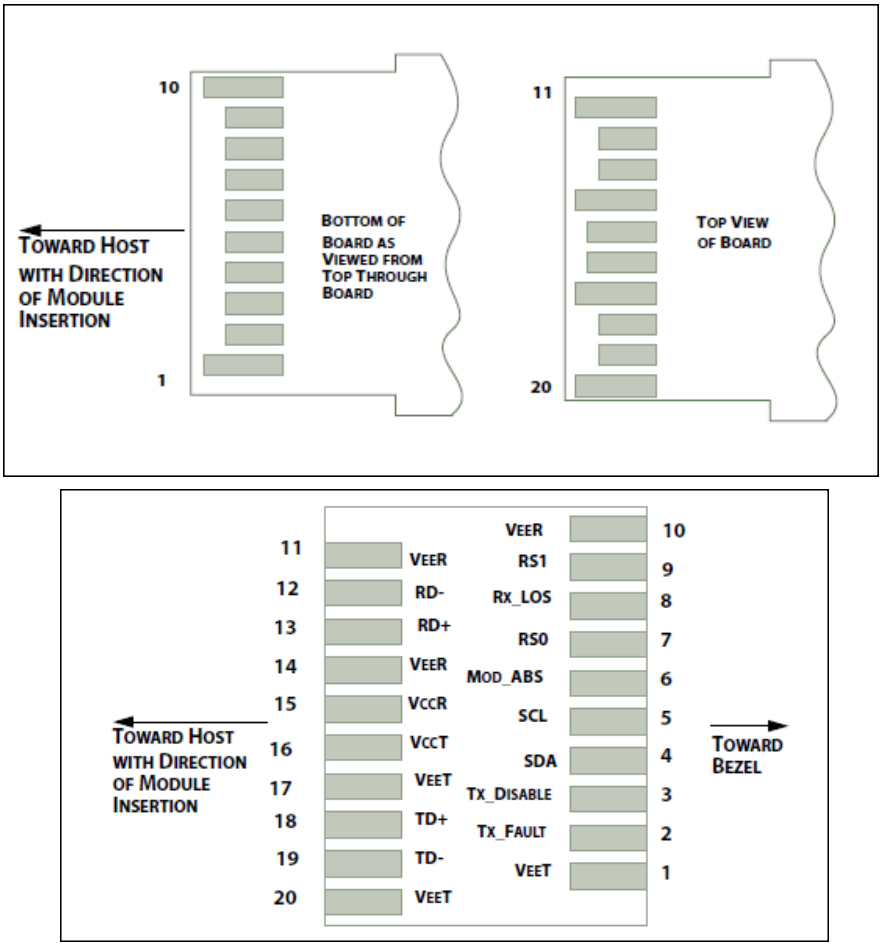


Figure 7: SFP56 Module Pin Map

4. High Speed Signals

High speed signals are electrically looped back from TX side to RX side of the module, the differential TX pair is connected to the corresponding RX pair, and the signals are AC coupled as specified by SFP MSA HW specs.

The Passive traces connecting TX to RX pairs are designed to support a data rate up to 56Gbps with minimal insertion loss.

5. Mechanical and thermal specifications

5.1 PCB outline

The PCB outline has been extended to the full size of the shell as shown in figure 8 below.

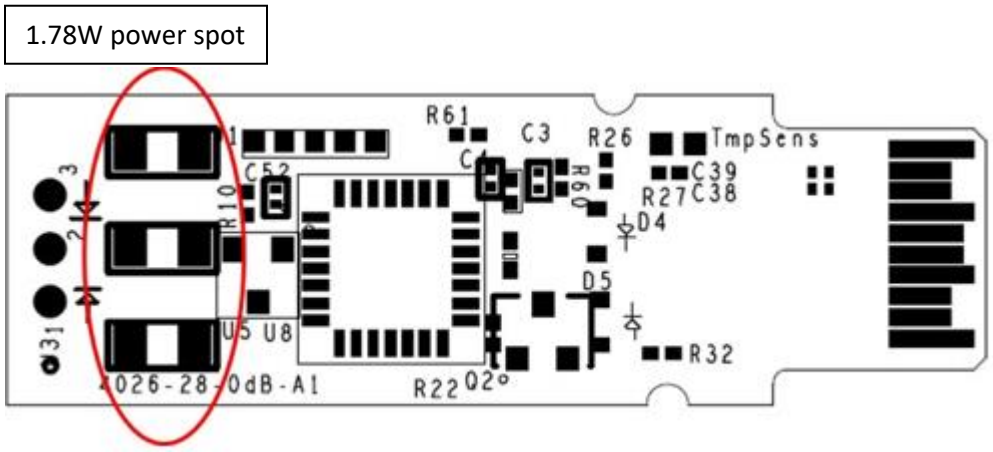


Figure 8: PCB outline top view

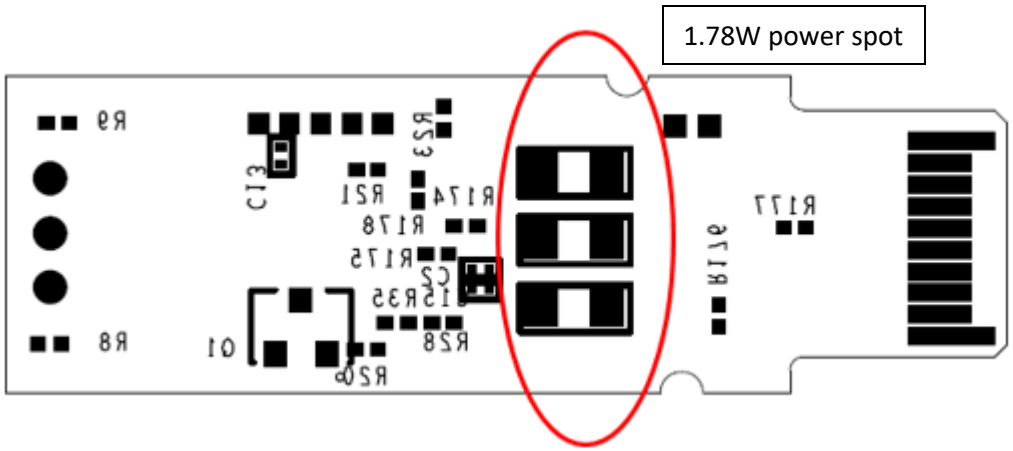


Figure 9: PCB outline bottom view

5.2 Thermal specifications

For a better thermal transfer and for reducing the thermal resistance between the PCB and the shell, a thermal pad is placed between the heated spots and the PCB shell in order to enhance the thermal conductance between the PCB and the shell.

5.3 SFP Shell

The SFP56 shell used is compliant with SFF-8432, it comes with N6 finish and a flat top for low thermal resistance and maximum heat transfer from the module to the heat sink.

Revision History

Revision number	Date	Description
0.1	2/12/2021	▪ Preliminary